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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,784	06/20/2001	Mong-Song Liang	67,200-327	3661

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/885,784	Applicant(s) LIANG ET AL.	
	Examiner Julio J. Maldonado	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,12,13 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8,12,13 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's cancellation to claim 11 is acknowledged.

2. Applicants' addition to claim 16 is acknowledged.

3. A new 103(a) rejection is made as set forth in this Office Action.

4. Claims 2-8, 12-13 and 16 are pending in this application.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3-7, 12-13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (U.S. 6,143,117) in view of Mountain (U.S. 6,013,534) and Haq (U.S. 6,245,677).

In reference to claim 16, Kelly et al. (Figs. 1-8) in a related method to transfer thin film structures teach the steps of providing a first semiconductor substrate (40); forming over the first semiconductor substrate (40) at least one microelectronic device (44) to form from the first semiconductor substrate (40) a partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46); providing a second substrate (10); forming over the second substrate (10), in inverted order, a dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46);

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the second substrate (10) to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication (44, 46, 20, 26, 32, 34, 36, 38); and removing the second substrate (10) from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication (44, 46, 20, 26, 32, 34, 36, 38) while employing a dicing method (column 4, line 55 – column 9, line 43).

Kelly et al. fail to teach removing said second substrate while employing the dielectric isolated metallization pattern as an etch stop layer. However, Mountain (Figs.10 and 11) in a related method to form a packaged structure teaches removing a substrate using a dielectric layer as a stop layer with a combination of chemical and mechanical processes (column 5, lines 6-13 and column 6, line 65 – column 7, line 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to remove the second a substrate down to a stop layer as taught by Mountain and using it as part of the dielectric isolated metallization pattern of the mounting method of Kelly et al., since this is a conventional process that can be used to reduce the thickness of the device and provide better handling (column 1, lines 36-47 and column 6, line 65 – column 7, line 3).

The combined teachings of Kelly et al. and Mountain fail to teach removing the second substrate from the laminated completely fabricated semiconductor integrated

circuit microelectronic fabrication while employing a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing method. However, Haq (Fig.1) in a related method to remove substrates teaches removing a substrate (step 4) using a method selected from the group consisting of milling methods, polish methods and chemical mechanical polish (CMP) planarizing method (column 2, line 55 – column 4, line 9). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to remove the substrate using the polishing method of Haq in the mounting method of Kelly et al. and Mountain, since by this manner it would reduce stress forces to the wafer during manufacturing (column 2, lines 66-67).

In reference to claims 3-6, and 12-13 Kelly et al. show that the second substrate (10) is selected from the group consisting of conductor substrates, semiconductor substrates and aggregates thereof; that the second substrate (10) is a second semiconductor substrate; that the first semiconductor substrate (40) is thicker than the second substrate (10); that the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) comprises a plurality of laminated patterned conductor layers; that the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) formed over the second substrate (10) is undertaken while employing a laminating method consisting of thermally assisted laminating; removing from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication (44, 46, 20, 26, 32, 34, 36, 38) the second substrate (10); that the semiconductor substrate is not

thinned after forming thereover the minimum of one microelectronic device; and that the second substrate (10) is not removed from the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication (44, 46) with the dielectric isolated metallization pattern (20, 26, 32, 34, 36, 38) (column 4, line 55 – column 9, line 43).

In reference to claim 7, Kelly et al. in combination with Mountain and Haq show all aspects of the invention but fails to teach that each laminated patterned conductor layer within the plurality of laminated patterned conductor layers is formed to a thickness of from about 3,000 to about 6,000 Å. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. ('117) in view of Mountain ('534) and Haq ('677) as applied to claims 3-6, 12-13 and 16 above, and further in view of Davidson (U.S. 5,880,010).

Kelly et al. in combination with Mountain and Haq substantially teach all aspects of the invention but fail to teach that the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors. However, Davidson in a related method to form packaging structures teach that the microelectronic device (i.e. the active layer) is selected from the group consisting of resistors, transistors, diodes and capacitors (column 3, lines 58-67).

Therefore, it would have been obvious to skilled in the art at the time of the invention was made to incorporate the microelectronic devices as taught by Davidson in the packaging structure of Kelly et al., Mountain and Haq, since by integrating the microelectronic device in the packing structure would reduce the space of an integrated circuit to less than 1% of its conventional size (column 1, lines 35-39).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. ('117) in view of Mountain ('534) and Haq ('677) as applied to claims 3-6, 12-13 and 16 above, and further in view of Davidson (U.S. 5,880,010).

Kelly et al. in combination with Haq and Mountain fail to teach using thermally assisted laminating methods and pressure assisted lamination methods to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern using a bonding material selected from the group consisting of indium and indium alloy bonding materials. However, Kresge et al.

(Fig.11) in a related method to form multilayered circuit boards, teach using pressure and temperature lamination methods using a bonding material selected from the group consisting of indium and indium alloy bonding materials (column 7, line 45 – column 8, line 35). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to adopt the pressure bonding lamination method using indium or indium alloy as bonding material as taught by Kresge et al. in the mounting method of Kelly et al., Mountain and Haq, since this would promote an effective engagement between the integrated circuits, and prevent dielectric intrusion through the conductive bond (column 8, lines 9-35).

Response to Arguments

9. Applicant's arguments filed 04/22/2003 have been fully considered but they are not persuasive.

Applicants argue, "...Haq's invention is rendered inoperative for its intended purpose since such complete thinning and removal of Haq's semiconductor substrate would also remove Haq's semiconductor devices and render inoperative Haq's live circuits...". In response to this argument, applicants assert that if this semiconductor substrate of Haq were completely removed would render the invention inoperative. However, Haq was relied on thinning semiconductor substrates using chemical mechanical polishing processes.

Also, applicants argue, "...Mountain's etch stop layer does not comprise a dielectric isolated metallization pattern employed within a semiconductor integrated circuit microelectronic fabrication...". In response to this argument, page 16 of the

submitted specification teaches a dielectric isolated metallization pattern (46) comprising a series of metal patterns and dielectric layers including a blanket terminal passivation layer (32) used as an etch stop layer, wherein this passivation layer comprises silicon nitride. The etch stop layer does not comprise a dielectric isolated metallization pattern. The dielectric isolated metallization pattern comprises an etch stop layer. Also, Mountain teaches depositing an etch stop layer comprising silicon nitride, as part of the conventional process that can be used to reduce the thickness of the device and provide better handling (Mountain, column 1, lines 36-47 and column 6, line 65 – column 7, line 3). Also, Mountain wasn't relied on providing a dielectric isolated metallization pattern. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
6/16/03

George Fourson
Primary Examiner